

Debug Port Requirements for Pentium® II/III Processors

An Application Note

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The following is American Arium's recommendation for implementation of a Pentium® II target debug port.

Debug Port Signal Description

Signal	Pin	Dir	Description	Suggested Termination
TDO	10	O	TAP Data Out (From last processor of scan chain to ITP port)	See below Note 1
TDI	8	I	TAP Data In (ITP port to first processor of scan chain)	See below Note 1
TMS	7	I	TAP Mode Select	See below Note 3
TCK	5	I	TAP Clock. Of the ITP signals, this is the most critical signal.	See below Note 2
TRST#	12	I	TAP Reset	470Ω to ground
BSEN#	14	I	Boundary scan (TAP) enable. ICE has access to TAP signals of CPU when low	See below Note 7
PRDY0#	18	O	Processor PRDY signal. From 1 st processor in single/multiprocessor system.	See below Note 4
PRDY1#	22	O	Processor PRDY signal. From 2 nd processor in a multiprocessor system.	See below Note 4
PRDY2#	26	O	Processor PRDY signal. From 3 rd processor in a multiprocessor system.	See below Note 4
PRDY3#	30	O	Processor PRDY signal. From 4 th processor in a multiprocessor system.	See below Note 4
PREQ0#	16	I	Processor PREQ signal. To 1 st processor in a single/multiprocessor system.	See below Note 5
PREQ1#	20	I	Processor PREQ signal. To 2 nd processor in a multiprocessor system.	See below Note 5
PREQ2#	24	I	Processor PREQ signal. To 3 rd processor in a multiprocessor system.	See below Note 5
PREQ3#	28	I	Processor PREQ signal. To 4 th processor in a multiprocessor system.	See below Note 5
RESET#	1	O	Processor RESET signal.	See below Note 6
DBRESET#	3	I	ICE reset output. When driven low, the target should reset the system and CPU.	240Ω to VCC (2.5V)
DBINST#	11	I	ICE installed. Debug cable grounds this signal, allowing target to detect the ICE.	See below Note 7
VTT	9	O	Target VTT. The ICE uses this to detect target power and establish GTL+ threshold.	1KΩ to VTT (1.5V)
BCLK	29	O	Private copy of BCLK that allows the ICE to provide a TCK that is synchronous with BCLK. In virtually all cases, a synchronous TCK is NOT used or required.	Best connected to Gnd in most cases
GND	2, 4, 6, 13, 15, 17, 19, 21, 23, 25, & 27		Signal grounds. Pin 2 (or sometimes 13) is unique in that it is sensed to determine if a target is attached.	Connect to ground

The resistor values given are typical values. Actual values are dependent on the target layout.

Dir (Signal Direction) is relative to target board. O (Out) is from target to ITP port. I (In) is from ITP port to target.

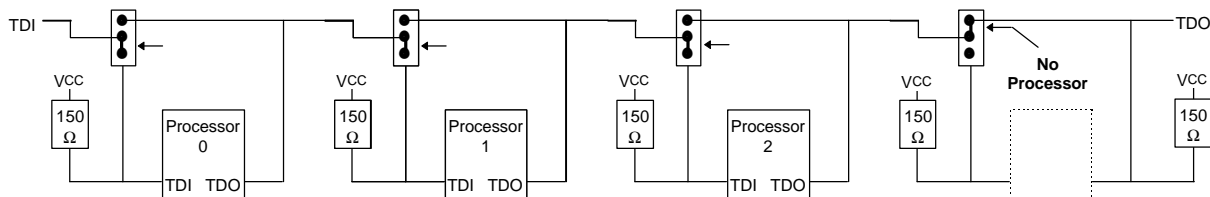
The Debug Port connection is achieved by way of a 30-pin connector specified as an AMP 104068-3. The pinout and suggested circuitry are fully described in the 1995 edition of the Pentium® Pro Processor Family User's Manual, Volume 1: Specifications, chapters 10 and 16 from Intel Corporation.

The Joint Test Action Group (JTAG) bus for on-module testing is defined in "Test Access Port and Boundary-Scan

Architecture, IEEE 1149.1-1990, 21 May 1990."

Note 1:

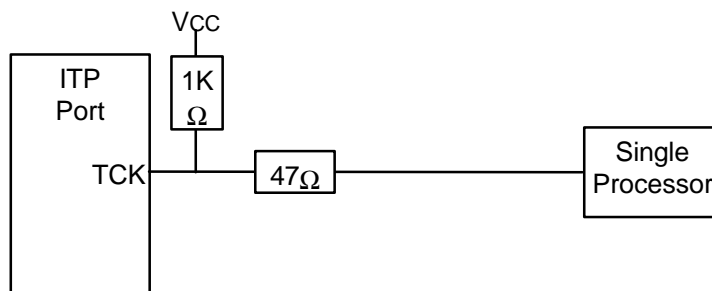
The TDO pin on each processor requires a 150Ω pull up resistor to VCC (2.5V). Bypassing TDI to TDO using a jumper when a processor socket is not populated must not result in more than one pull up resistor on any TDO output. The jumper implementation shown below will accomplish this and insure that there is only one pull up on each TDO.



Note 2:

Single Processor

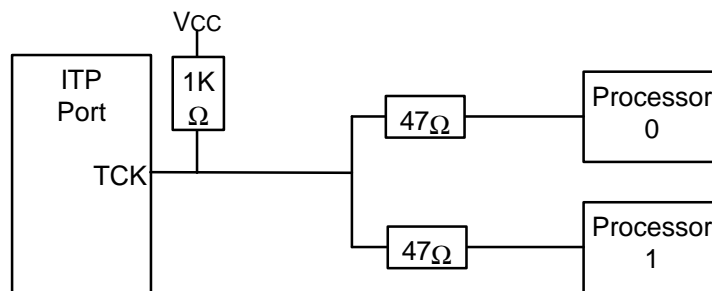
TCK is the most critical of the ITP signals. In the case of a single processor, TCK may be pulled up to VCC (2.5V) through a 1K ohm resistor and then passed through a 47 ohm series resistor before being routed to the processor as shown in the following figure.



Note 2:

Dual-Processor

TCK is the most critical of the ITP signals. In the case of a two processor system, TCK may be pulled up to VCC (2.5V) through a 1K ohm resistor and then passed through separate 47 ohm series resistors to each of the processors as shown in the following figure.

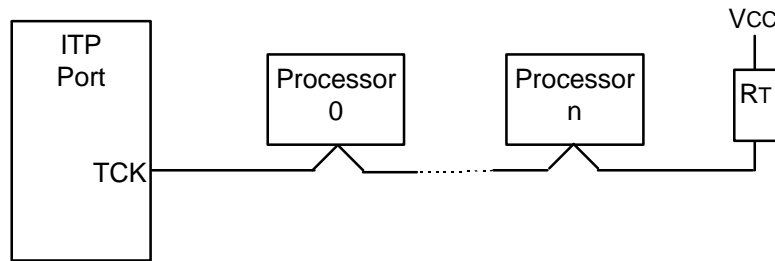


Note 2 (con't):

Multiprocessor

TCK is the most critical of the ITP signals. The best approach for a multiprocessor system is to provide a separately buffered copy of this signal that is properly terminated to each device. Termination on each buffered copy would be similar to the single processor method show earlier.

The second best approach is to implement TCK as a daisy chain to each processor with a 62 to 100 ohm terminating resistor to VCC (2.5V) at the terminal end (located farthest from the debug port). The actual R value depends on the trace impedance of the target.

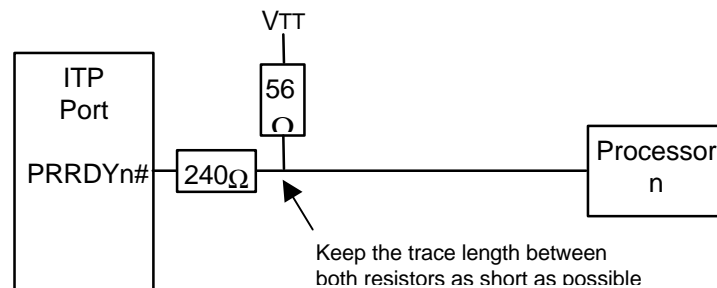


Note 3:

TMS can be routed similar to the daisy chain method shown above for TCK. Some early American Arium products such as the ICE-I6ECM and the POD-I6 may not be able to properly drive TMS when R_T is less than 180 ohms.

Note 4:

All four PRDYn# signals are GTL+ signals and should be end terminated to VTT (1.5V) through a 56Ω resistor on the target. The signal supplied to the debug port should pass through a 240 ohm series resistor located as close as possible to the pull-up resistor. Do not add any stubs off of these traces. End termination resistor values for GTL signals vary according to the effective trace impedance and VTT power dissipation issues.

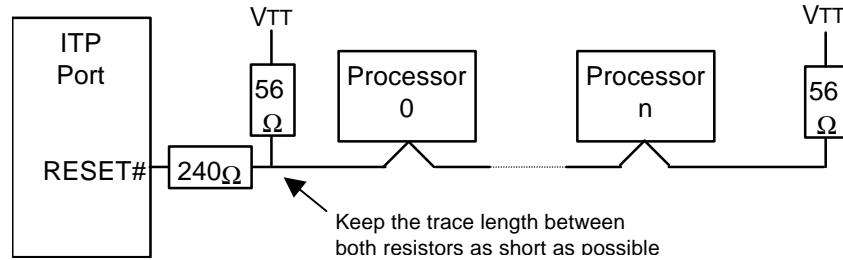


Note 5:

PREQn# signals should be pulled up to VCC (2.5V) in the range of 270 ohms to 10K ohms on the target.

Note 6:

RESET# is a GTL+ signal and should be terminated to VTT (1.5V) through 56Ω resistors at both ends of the signal. The signal supplied to the debug port should pass through a 240 ohm series resistor located as close as possible to the nearest terminated end. Do not add any stubs off of this trace.



Note 7:

BSEN# and DBINST# should be pulled up to VCC with a 10K resistor if this signal is used by the target. Otherwise, it may be left open.



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